AMENDMENTS TO THE DRAWINGS

The Patent Office objects to the Drawings under 37 C.F.R. § 1.83(a) as not including every feature of the invention, *i.e.*, the recitation of "a stage of varying charging or discharging speed of the capacitor by shifting switching control timings in switches in said switch group" is not shown in the Drawings.

Applicant submits that the amendment to claim 7 has obviated this rejection, and requests withdrawal of the § 1.83(a) objection to the Drawings.

The Patent Office objects to Figure 6, since the output of the NOR gate (IN2.IN1D.NOR) and the output of the NAND gate (IN2.IN2D.NAND) are left "dangling."

The function of the outputs of the NOR and NAND gate are shown in the switch timing waveforms of Figure 7, and the output of the NOR gate (IN2.IN1D.NOR) and the output of the NAND gate (IN2.IN2D.NAND) serve to illustrate how the delay elements DL1 and DL2 affect the switch timing. Furthermore, in actual fabrication, these dummy gates would be used for capacitance equalization purposes. Applicants herein amend Figure 7 to further clarify the timing relationships between the input signals and the NAND and NOR gates. No new matter has been added.

Attachment: Fifty-two (52) Replacement Sheets

REMARKS

Claim 7 has been examined on its merits, and is the only claim presently pending in the application.

1. Claim 7 stands rejected under 35 U.S.C. § 112 (2nd para.) as allegedly being indefinite. Applicant traverses the § 112 (2nd para.) of claim 7 for at least the reasons discussed below.

Applicant submits that the § 112 (2nd para.) of claim 7 is now moot, since amended claim 7 no longer recites a "a stage of varying charging or discharging speed of the capacitor by shifting switching control timings of switches in said switch group." Thus, Applicant submits that § 112 (2nd para.) of claim 7 has been overcome, and respectfully requests reconsideration and withdrawal of same.

In response to the Patent Office's argument that DL1 and DL2 will not vary the charging or discharging speed of the capacitor C by shifting the switch control timings, Applicant submits that the Patent Office is mistaken. For example, the charging speed of the capacitor C is determined by whether only MP1 is turned on, only MP2 is turned on or both MP1 and MP2 are turned on. In the instant written disclosure, the function of the delay elements DL1 and DL2 is described, along with their effect on the charging/discharging of the capacitor C. *See, e.g.*, page 24, line 17 to page 25, line 19. Furthermore, it is plainly evident from Figure 7 that, without the delay elements DL1 and DL2, the control signals output from the NAND and NOR gates would be completely different.

2. Claim 7 stands rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Fujiwara (U.S. Patent No. 6,225,844). Applicant traverses the § 102(e) rejection of claim 7 for at least the reasons discussed below.

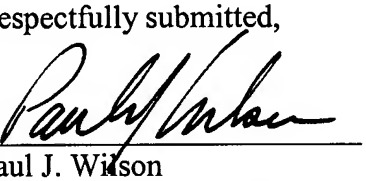
First, the Patent Office alleges that Fujiwara discloses a stage to which a plurality of clocks having mutually different phases are input, and the Patent Office points to the stage IN of Figure 1 of Fujiwara. However, the stage IN of Fujiwara accepts only a single clock, which is then buffered by two inverters IV1 and IV2 to create the signals IB and IBB. Therefore, assuming *arguendo* that the signals IB and IBB could be considered to be the control signals recited in claim 7, the phase difference between the two control signals (any phase difference would be based solely on the switching time of the inverter circuits) would remain constant. If the phase difference between the signals IB and IBB remains constant, then the switch control timings of the switch group (identified by the Patent Office as P1, P101, P102, N101) cannot be shifted to vary the charging and/or discharging speed of the capacitor C101.

Based on the foregoing reasons, Applicant submits that Fujiwara fails to teach or suggest all of the claimed elements as arranged in claim 7. Thus, Applicant submits that claim 7 is allowable, and respectfully request that the Patent Office reconsider and withdraw the § 102(e) rejection of claim 7.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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